IN THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Canceled)

2. (Canceled)

3. (Previously Presented) A method of forming an interlayer dielectric film in a semiconductor device, the method comprising:

forming conductive layer pattern on a semiconductor substrate including a junction region and an isolation region;

forming insulating film spacers on sidewalls of said conductive layer pattern to expose the junction region;

burying a conductive material between said insulating film spacers;

removing said conductive material and said insulating film spacers in the isolation region; and

forming an interlayer dielectric film on an entire surface of the semiconductor device so that the interlayer dielectric film is buried between the conductive layer pattern in the isolation region .

4. (Currently Amended) The method of according to claim 3, wherein said conductive layer pattern includes a word line or a bit line.

5. (Canceled)

6. (Canceled)

7. (Currently Amended) A method of forming an interlayer dielectric film in a semiconductor device, the method comprising:

forming conductive layer patterns and an insulating film spacers on sidewalls of said conductive layer patterns on a semiconductor substrate to expose a first contact plug;

~~burying a~~ forming a conductive material on the entire surface to bury the conductive material between said insulating film spacers;

removing said conductive material and the insulating film spacers at a removal region such that said conductive material remains on the first contact plug to form a second contact plug and the insulating film spacers only remain at both ~~side~~ sides of the second contact plug; and

burying an interlayer dielectric film between said conductive layer patterns at said removal region.

8. (Previously Presented) The method according to claim 7, wherein said conductive layer pattern includes a bit line.

9. (Currently Amended) A method of forming an interlayer dielectric film in a semiconductor device, the method comprising:

forming first conductive layer patterns on a semiconductor substrate including a junction region and an isolation region;

forming first spacers on sidewalls of the first conductive layer patterns;

removing the first spacers on the isolation region;

forming a first interlayer dielectric film on the entire surface;

forming a first contact hole by patterning the first interlayer dielectric film to expose the junction region;

forming a first contact plug by burying a first conductive material in the first contact hole;

forming second conductive layer patterns on the entire surface including the first contact plug;

forming second spacers on sidewalls of the second conductive layer patterns;

forming a second conductive material on the entire surface to bury the second conductive material between the second conductive patterns;

forming a second contact plug by remaining the second conductive material on the first contact plug and removing the second conductive material and the second spacers on the first interlayer dielectric film, wherein the second spacers remains at both side of the second contact plug; and

forming a second interlayer dielectric film on the entire surface;

10. (Previously Presented) The method according to claim 9, wherein the first conductive layer patterns comprises a word line.

11. (Previously Presented) The method according to claim 9, wherein the second conductive layer patterns comprises a bit line.

12. (Previously Presented) The method according to claim 9, wherein the second conductive material includes a polysilicon.

13. (Previously Presented) The method according to claim 9, wherein the second conductive layer patterns further includes nitride film.

14. (Previously Presented) The method according to claim 9, the method further comprising:

performing a first planarization process to remove the second conductive material on the second conductive patterns after forming the second conductive material.

15. (Previously Presented) The method according to claim 9, the method further comprising:

performing a second planarization process after forming the second interlayer dielectric film on the entire surface.

16. (Previously Presented) The method according to claim 9, wherein the first spacers is remained at both side of the first contact plug.